What is claimed is:

1. A flat panel display device, comprising:

a semiconductor layer formed on an insulating substrate;

source and drain electrodes directly contacting a first end portion and a second end portion of the semiconductor layer, respectively;

a pixel electrode having an opening portion formed thereon;

a first insulating layer formed over the remaining portion of the insulating substrate except for the opening portion;

a gate electrode formed on a portion of the first insulating layer formed over the semiconductor layer; and

source and drain regions formed in the first end portion and the second end portion of the semiconductor layer.

2. The device of claim 1, wherein the source and drain electrodes include a pixel electrode material layer, a metal material layer, and a capping insulating material layer, each stacked sequentially.

3. The device of claim 2, wherein the pixel electrode extends from either of the source and drain electrodes.

4. The device of claim 2, further comprising, a storage capacitor including first and second capacitor electrodes with a dielectric layer interposed therebetween, the first capacitor electrode including the pixel electrode material layer and the metal material layer, each stacked sequentially, the second capacitor electrode including a gate electrode material layer, the dielectric layer including the capping insulating material layer and the first insulating layer, each stacked sequentially.

5. The device of claim 1, wherein the source and drain regions include an offset region formed in a portion of the semiconductor layer between the source and drain electrodes and the gate electrode.

6. The device of claim 1, wherein the source and drain regions include low-density source and drain regions formed in a portion of the semiconductor layer between the source and drain electrodes and the gate electrode, thereby forming a lightly doped drain structure.

7. The device of claim 1, further comprising, first and second spacers, the first spacer formed on side wall portions of the source and drain regions, the second spacer formed on side wall portions of the gate electrode and the opening portion.

8. The device of claim 1, further comprising, a second insulating layer for planarization on the remaining portion of the first insulating layer except for the opening portion.

9. The device of claim 1, wherein the gate electrode includes a metal material layer and a capping insulating layer, each stacked sequentially.

10. A method of manufacturing a flat panel display device, comprising:

forming a semiconductor layer on an insulating layer;

ion-implanting an impurity having a first conductivity into the semiconductor layer;

forming source and drain electrodes, the source and drain electrodes directly contacting a first end portion and a second end portion of the semiconductor layer;

ion-implanting an impurity having a second conductivity into the semiconductor layer to form high-density source and drain regions and a channel area, the high-density source and drain regions directly contacting the source and drain electrodes;

forming a first insulating layer over an entire surface of the insulating substrate;

forming a pixel electrode having an opening portion formed thereon; and

forming a gate electrode on a portion of the first insulating layer formed over the semiconductor layer.

11. The method of claim 10, wherein the source and drain electrodes include a pixel electrode material layer, a metal material layer and a capping insulating material layer, each stacked sequentially.

12. The method of claim 10, wherein the pixel electrode exposed through the opening portion is formed by sequentially etching the first insulating layer, a capping insulating layer and a metal material layer, each stacked sequentially.

13. The method of claim 12, further comprising, a storage capacitor including first and second capacitor electrodes with a dielectric layer interposed therebetween, the first capacitor electrode extending from either of the source and drain electrodes and including the pixel electrode material layer and the metal material layer, each stacked sequentially, the second capacitor including a gate electrode material layer, the dielectric layer electrode formed on the first capacitor electrode and including the capping insulating layer and the first insulating layer, each stacked sequentially.

14. The method of claim 13, further comprising, forming a contact hole contemporaneously with forming the pixel electrode having the opening portion, the contact hole contacting the first capacitor electrode and the gate electrode.